ACS APPLIED MATERIALS & INTERFACES

Research Article

www.acsami.org

Synergistic Approach to High-Performance Oxide Thin Film Transistors Using a Bilayer Channel Architecture

Xinge Yu,[†,‡] Nanjia Zhou,[‡] Jeremy Smith,[‡] Hui Lin,[†,‡] Katie Stallings,[‡] Junsheng Yu,[†] Tobin J. Marks,*[,‡] and Antonio Facchetti*[,‡,§]

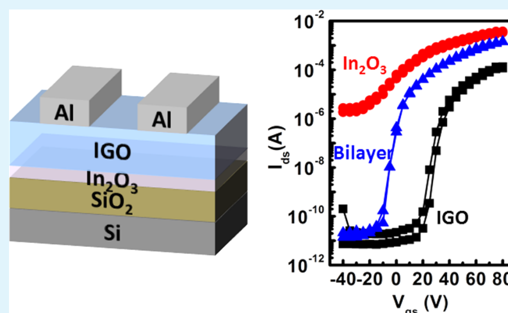
[†]State Key Laboratory of Electronic Thin Films and Integrated Devices, School of Optoelectronic Information, University of Electronic Science and Technology of China (UESTC), Chengdu 610054, P. R. China

[‡]Department of Chemistry and the Materials Research Center, Northwestern University, 2145 Sheridan Road, Evanston, Illinois, 60208, United States

[§]Polyera Corporation, 8045 Lamon Avenue, Skokie, Illinois, 60077, United States

Supporting Information

ABSTRACT: We report here a bilayer metal oxide thin film transistor concept (bMO TFT) where the channel has the structure: dielectric/semiconducting indium oxide (In_2O_3) layer/semiconducting indium gallium oxide (IGO) layer. Both semiconducting layers are grown from solution via a low-temperature combustion process. The TFT mobilities of bottom-gate/top-contact bMO TFTs processed at T = 250 °C are ~5tmex larger (~2.6 cm^2/(V s)) than those of single-layer IGO TFTs (~0.5 cm^2/(V s)), reaching values comparable to single-layer combustion-processed In_2O_3 TFTs (~3.2 cm^2/(V s)). More importantly, and unlike single-layer In_2O_3 TFTs, the threshold voltage of the bMO TFTs is ~0.0 V, and the current on/off ratio is significantly enhanced to ~1 × 10^8 (vs ~1 × 10^4 for In_2O_3). The microstructure and morphology of the In_2O_3/IGO bilayers are analyzed by X-ray diffraction, atomic force microscopy, X-ray photoelectron spectroscopy, and transmission electron microscopy, revealing the polycrystalline nature of the In_2O_3 layer and the amorphous nature of the IGO layer. This work demonstrates that solution-processed metal oxides can be implemented in bilayer TFT architectures with significantly enhanced performance.



KEYWORDS: *thin film transistor (TFT), indium oxide, indium gallium oxide, bilayer structure*

INTRODUCTION

Thin film transistors based on metal oxide semiconductors (MO TFTs) have attracted considerable attention because of their high carrier mobilities, high optical transparency, and environmental stability.[1−5] Thus, they are being actively investigated as replacements for silicon-based TFTs in the back-planes of next-generation liquid crystal (LC) and active matrix organic light-emitting diode (AMOLED) displays.[6−9] Among metal oxide semiconductors, amorphous oxides are the most promising candidates for large-area TFT applications because of their grain-boundary free thin film properties,[1−5,10−14] with ZTO,[15,16] IZO,[17,18] IGO,[19] and IGZO.[2,20−22] being the most investigated.

Proper attention to device structure design and materials integration are crucial for optimizing TFT performance. In particular, bilayer metal oxide TFTs (bMO TFTs), where two metal oxide films are used as the channel layer, offer significant performance advantages by combining the properties of two semiconducting materials. Recently, bMO TFTs based on IZO/HIZO[23] and IZO/IGZO[24] as the channel layer have been reported, exhibiting carrier mobilities of 48 and 30 cm^2/(V s), respectively, and good on−off ratios (1 × 10^8 to 1 × 10^{10}). Furthermore, when compared to the corresponding IZO single layer devices, these bilayer devices effectively enhance the photostability[23] and suppress normalized current noise spectral density.[24] To date, the predominant techniques for depositing such bilayer oxide films have been vapor-phase processes. However, solution-based growth processes are attractive because they can be carried out at low temperatures compatible with plastic substrates, offer the possibility of large-scale cost-effective roll-to-roll manufacture, and avoid capital-intensive vacuum equipment.[25] Recently, this laboratory reported a new methodology to fabricate MO TFTs from solution and at low temperature via "combustion synthesis."[26,27] With this approach, a variety of MO-based TFTs, including In_2O_3 devices with mobilities ~1 cm^2/(V s) can be fabricated on Si/SiO_2 at temperatures as low as 200 °C. However, despite the good In_2O_3 mobility (μ), facile crystallization of this material under the combustion synthesis conditions, the yields TFTs exhibit less than optimum current modulation (I_{on}/I_{off}) and threshold voltage (V_T) uniformity over large areas.[27,28] In contrast, amorphous oxides such as IGZO, IZO, and IGO can be prepared via low-temperature combustion techniques[26,27] and

Received: May 29, 2013
Accepted: July 22, 2013
Published: July 22, 2013

 © 2013 American Chemical Society

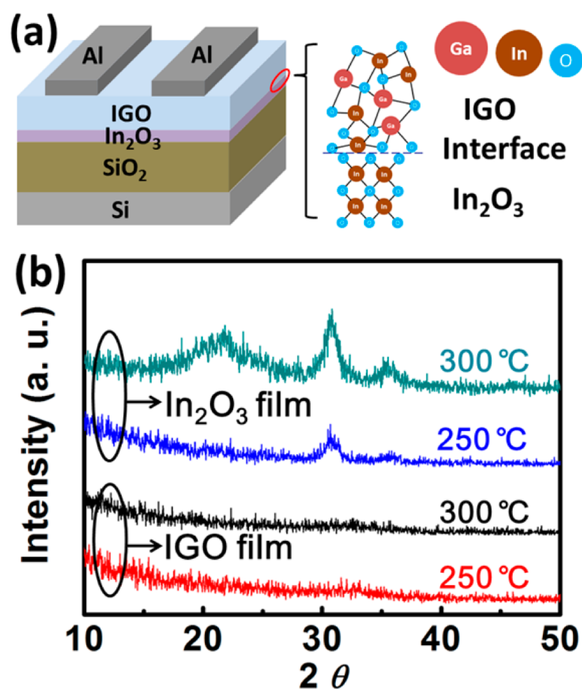


Figure 1. (a) In_2O_3/IGO bMO TFT device architecture employed in this study and schematic representation of a metal oxide lattice. (b) θ–2θ XRD scans of 15 nm In_2O_3 and IGO films deposited on SiO_2 substrates and annealed at the indicated temperatures.

have more controllable carrier densities with minimal grain boundary effects.[2,18,26,28] However, the electron mobilities for these materials are typically lower than those obtained for combustion-derived In_2O_3 (5–8 cm^2/vs, T = 300 °C), and therefore the question arises as to whether it is possible to usefully combine the high field-effect mobility of a polycrystalline oxide with the carrier density control and film uniformity of an amorphous oxide, using an all-combustion process.

In this letter, we report novel In_2O_3/IGO bottom-gate top-contact bMO TFTs fabricated at low temperature. After optimizing In_2O_3/IGO film deposition by varying the film thicknesses and combustion processing parameters, the bilayer TFTs achieve greatly enhanced performance for 250 °C processing temperature ($\mu \approx 2.56$ cm^2/(V s), $I_{on}/I_{off} \approx 1 \times 10^8$, $V_T \approx +6.3$ V) compared to single-layer In_2O_3 ($\mu \approx 3.22$ cm^2/(V s), $I_{on}/I_{off} \approx 1 \times 10^4$, $V_T \approx -10.8$ V) or IGO ($\mu \approx 0.52$ cm^2/(V s), $I_{on}/I_{off} \approx 1 \times 10^7$, $V_T \approx +30.3$ V) devices. The morphology and microstructure of the bilayer films are characterized by atomic force microscopy (AFM), X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and transmission electron microscopy (TEM), evidencing a well-defined crystalline/amorphous bilayer microstructure.

EXPERIMENTAL SECTION

Precursor Solutions. Acetylacetone fuel-based In_2O_3 and Ga_2O_3 precursor solutions were prepared with $In(NO_3)_3 \cdot xH_2O$ and $Ga(NO_3)_3 \cdot xH_2O$ (IGO:0.65:0.35 mol ratio), dissolved in 2-methoxyethanol with acetylacetone and NH_4OH to yield 0.05 M a solution. All reagents were from Sigma-Aldrich and used as received. In_2O_3 precursor solutions were prepared similarly with concentrations ranging from 0.01 to 0.05 M for film thickness variation. Precursor solutions were stirred for more than 3 h at 25 °C before device fabrication.

Transistor Fabrication and Electrical Performance. Doped silicon substrates with a 300 nm thermal SiO_2 layers were used as the gate electrode and dielectric layer, respectively. In_2O_3 precursor solutions were spin-coated onto the SiO_2 at 3500 rpm for 35 s, and then annealed on a hot plate at temperatures ranging from 200 to 300 °C for 30 min. Subsequently, the 0.05 M IGO precursor solution was spin-coated onto the In_2O_3 channel film and annealed under the same conditions. This procedure was repeated for achieving the desired IGO thickness. Finally, 40 nm Al source and drain electrodes were thermally evaporated onto the IGO film through a shadow mask. The channel length and width for all devices in this study were 50 and 1000 μm, respectively. Similarly, TFTs with single In_2O_3 or IGO active layers (3× spin-coated layers) were fabricated for comparison.

Table 1. Performance Metrics of Single-Layer In_2O_3, IGO, and Bilayer In_2O_3/IGO TFTs with Different In_2O_3 Layer Thicknesses and Processing Temperatures

metal oxide	T_p (°C)	mobility (cm^2/(V s))	V_t (V)	log (I_{on}/I_{off})
In_2O_3 (15 nm)	200	0.63 ± 0.11	4.8 ± 3.6	6.2 ± 0.2
	250	3.22 ± 0.38	−10.8 ± 5.3	3.8 ± 0.3
	300	6.41 ± 0.71	−31.4 ± 6.5	3.0 ± 0.2
IGO (15 nm)	200	Inactive	—	—
	250	0.52 ± 0.19	30.3 ± 7.1	6.8 ± 0.1
	300	2.32 ± 0.0.34	15.1 ± 5.6	6.1 ± 0.2
In_2O_3 (1 nm)/IGO (10 nm)	200	Inactive (μ~10^{-5})		
	250	0.78 ± 0.23	25.5 ± 6.4	7.2 ± 0.3
	300	1.63 ± 0.57	17.3 ± 8.8	6.3 ± 0.3
In_2O_3 (2 nm)/IGO (10 nm)	200	10^{-3}	57.4 ± 9.7	4.9 ± 0.1
	250	1.39 ± 0.27	17.9 ± 3.2	7.4 ± 0.2
	300	2.95 ± 0.37	9.9 ± 6.1	6.6 ± 0.3
In_2O_3 (3 nm)/IGO (10 mn)	200	0.022 ± 0.0083	52.1 ± 7.5	5.4 ± 0.2
	250	2.56 ± 0.31	6.3 ± 3.7	7.9 ± 0.3
	300	3.71 ± 0.48	−3.7 ± 4.3	5.4 ± 0.1
In_2O_3 (4 nm)/IGO (10 nm)	200	0.27 ± 0.068	15.5 ± 6.8	5.8 ± 0.3
	250	2.87 ± 0.39	2.4 ± 4.7	5.8 ± 0.4
	300	5.21 ± 0.62	−18.6 ± 5.6	3.9 ± 0.3
In_2O_3 (5 nm)/IGO (10 nm)	200	0.36 ± 0.83	9.5 ± 7.8	6.2 ± 0.2
	250	3.01 ± 0.44	−1.1 ± 3.9	4.6 ± 0.3
	300	5.74 ± 0.74	−26.4 ± 7.7	3.5 ± 0.2

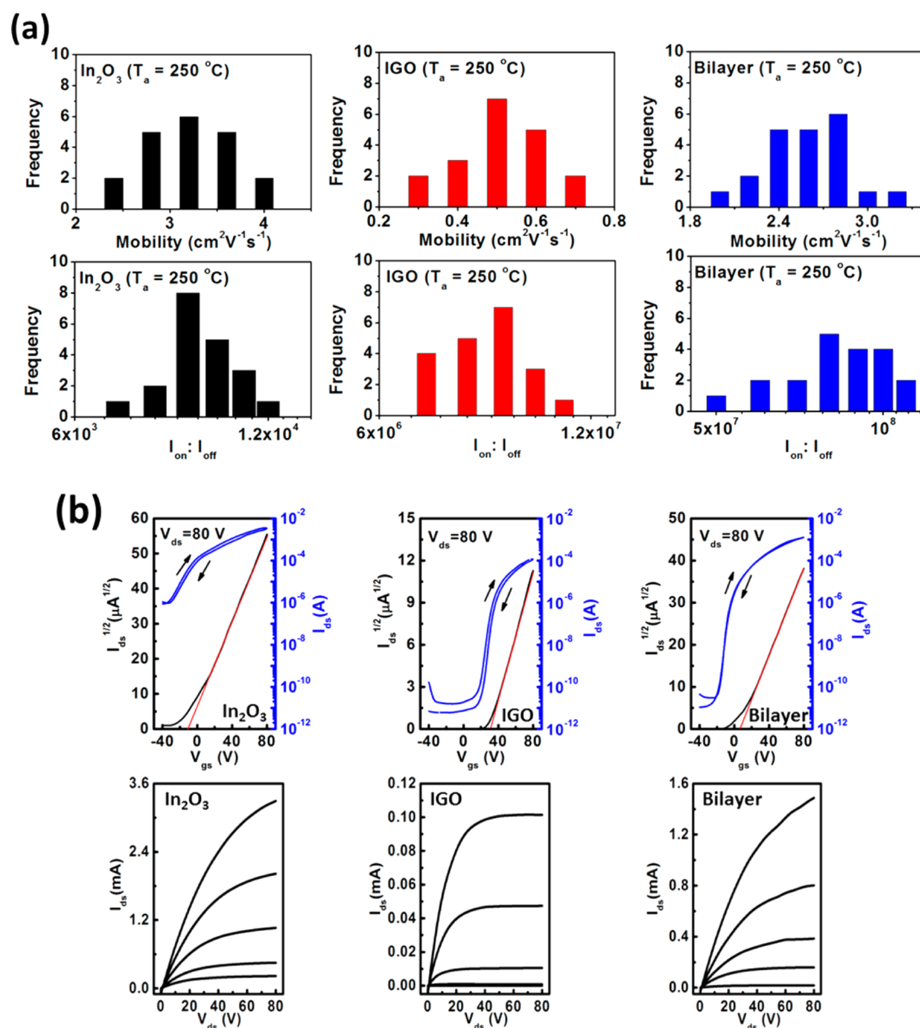


Figure 2. (a) Saturation TFT mobility and current on/off ratio plots for single layer In_2O_3 TFTs, single layer IGO TFTs, and bilayer In_2O_3 (3 nm)/IGO (10 nm) TFTs, processed at 250 °C. (b) Typical transfer (I_{DS}-V_{GS}) and output (I_{DS}−V_{DS}) plots of the indicated TFT devices: single-layer In_2O_3 TFT, single-layer IGO TFT, and bilayer In_2O_3 (3 nm)/IGO (10 nm) TFT annealed at T = 250 °C.

TFT characterization was performed under ambient conditions on a custom probe station using a Keithley 2400 sourcemeter and 6430 subfemtometer, operated by a locally written Labview program and GPIB communication. The charge carrier mobility μ was evaluated in the saturation region with the conventional MOSFET model in eq 1

$$I_{DS} = (WC_i/2L)\mu(V_{GS} - V_T)^2 \quad (1)$$

where C_i is the capacitance per unit area of insulator, V_T is the threshold voltage, and V_{GS} is gate voltage. W and L are channel width and length, respectively.

Oxide Film Characterization. Film morphologies were imaged with a Veeco Dimension Icon scanning Probe Microscope in tapping mode. XRD measurements were performed with a Rigaku ATX-G Thin Film Diffraction Workstation using Cu kα radiation coupled to a multilayer mirror. For cross-sectional TEM measurements, samples were prepared using focused ion beam (FIB) techniques (FEI Helios NanoLab 600). A thin Pt/Au layer was locally deposited on the sample to protect it from damage during the FIB processing. The prepared sample was then lifted with an OmniProbe nanomanipulator and transferred to a semispherical Cu TEM grid. TEM imaging was conducted with a JEOL-2100F microscope. XPS (Omicron ESCA Probe) depth profiling was performed on actual devices prepared without the top electrode. Samples were sputtered with an Ar^+ gun at 3000 eV and etched from the air/IGO interface.

RESULTS AND DISCUSSION

The device structure used in this study is shown in Figure 1a. Bottom-gate/top-contact (BGTC) TFTs were fabricated on Si/SiO_2 substrates on which the single- or bilayer metal oxide channel film is deposited via combustion synthesis at three different processing temperatures (200, 250, and 300 °C). Bilayer films with different In_2O_3 film thicknesses ranging from 1 to 5 nm were spin-coated onto the dielectric layer on top of which a 10 nm thick IGO (In:Ga = 65%:35%) layer was subsequently spun as the second layer. The devices were completed by thermally evaporating 40 nm thick Al source and drain electrodes. For comparison, control TFTs were fabricated using 15 nm thick single-layer In_2O_3 or IGO films (details in the Experimental Section).

Figure 1b shows XRD scans of 15 nm thick In_2O_3 and IGO films prepared at two processing temperatures, 250 and 300 °C. The relatively sharp reflections observed for In_2O_3 indicate polycrystalline film formation, irrespective of thickness, as evidenced by TEM energy-filtered nanobeamed diffraction (EF-NBD) of the thinner film, whereas the IGO films are amorphous.[26] We have fabricated at least 20 devices for each TFT structure, and the average TFT performance of these separately fabricated single-layer and bilayer TFTs for various

annealing temperatures is summarized in Table 1. The bilayer field-effect mobilities are far greater than those of the single-layer IGO TFTs, and even comparable to that of thick single-layer In_2O_3 devices. Furthermore, comparing to In_2O_3 TFT, the bilayer TFT V_T values shift to positive values, bringing V_T close to zero and providing high I_{on}/I_{off} ratios. The variation of mobility and I_{on}/I_{off} with In_2O_3 thickness for different processing temperatures is shown in the Supporting Information, Figure S1.

Films in which the first In_2O_3 layer (1−5 nm) is processed below 250 °C exhibit smooth, uniform morphologies with an RMS roughness <0.5 nm (see the Supporting Information, Figure S2). Note that the mobility of bilayer TFTs with an ultrathin (1 nm) In_2O_3 layer is lower than that of single-layer IGO devices processed at 300 °C. This result can be partially attributed to the increased conductivity of IGO films formed at higher processing temperatures.[26,30,31] Furthermore, the AFM images (Supporting Information, Figure S2) of In_2O_3 layers processed at 300 °C reveal that such ultrathin In_2O_3 films (1−2 nm) are uneven and discontinuous, which suggests trap sites, in accord with the low mobilities.[32−35]

After systematic optimization, bMO TFTs with a 3 nm In_2O_3 film and a 10 nm IGO layer exhibit the greatest performance (from Figure S1 in the Supporting Information, Figure 2a, and Table 1). Representative transfer and output plots for these bilayer devices versus those of the corresponding single-layer In_2O_3 (15 nm) and IGO (15 nm) devices processed at 250 °C are shown in Figure 2b. These data clearly show that single-layer In_2O_3 TFTs exhibit the highest saturation current (I_{sat}) of all devices for V_{DS} = +80 V and V_{GS} = +80 V, achieving an average mobility $\mu \approx 3.22$ cm^2/(V s). However, the threshold voltage (V_T) is negative, approximately −11 V, because of high carrier concentrations arising from the Fermi level proximity to the conduction band minimum (CBM).[27,28] Thus, it is difficult to deplete the carriers in the In_2O_3 films, yielding a negative V_T, high off-currents (I_{off}), and a low I_{on}/I_{off} ratio of only ~1×10^4. In contrast, single-layer IGO TFTs exhibit a very low I_{off} = ~1×10^{-12} A and a very large positive V_T, ~ +30 V. This can be explained by the O getter properties of Ga^{3+}, which can reduce the carrier concentration and increase empty traps,[29,30] leading to saturation of O gettering sites in IGO films upon completion of "combustion synthesis". Consequently, a larger gate voltage is required to induce more carriers to prefill the traps, leading to an increase of threshold voltage. Meanwhile, the device I_{off} and I_{sat} decrease, leading to a large I_{on}/I_{off} of ~1×10^6, but also to a lower μ of ~0.52 cm^2/(V s).

However, by combining the In_2O_3 TFT high I_{sat} and μ, with the IGO TFT high V_T and I_{on}/I_{off}, the resulting bilayer In_2O_3/IGO TFTs show a remarkable I_{sat} of ~1.5 mA (at $V_{DS} = V_{GS}$ = 80 V), more than 10x higher than that of a single-layer IGO device ($I_{sat} \approx 0.1$ mA), reaching a value only slightly below that of a single In_2O_3 active layer TFT (I_{sat} = 3.3 mA). In addition, the bilayer TFT exhibits a notable μ of ~2.6 cm^2/(V s) (average value) and V_T is close to 0.0 V. The low I_{off} is nearly identical to that of single-layer IGO TFTs, affording a high I_{on}/I_{off} of ~1×10^8. This is attributed to the carriers in the In_2O_3 channel layer prefilling empty IGO film traps.[28,30] On the opposite, bilayer TFTs with thicker In_2O_3 channel layers show negative V_T and low I_{on}/I_{off}, which is caused by the uncalled free carriers induced by In_2O_3 films.

XPS with depth profiling was used to analyze the O1s core levels in the In_2O_3 (3 nm)/IGO (10 nm) bilayers. Generally, O1s features at 529.9, 531.4, and 531.7 eV are assigned to oxide lattices without oxygen vacancies, with oxygen vacancies, and with metal hydroxide species, respectively. The additional peak at 532.3 eV is assignable to adsorbed oxygen species (for example, H_2O, CO_2).[36−39] In these bilayers, the O1s binding energy shows an abrupt shift to higher energies after the films are ion-gun-bombarded for various times (see the Supporting Information, Figure S3). And the distinct transition from the upper IGO to the lower In_2O_3 channel layers is evident from the shift of the In and O binding energies in the In_2O_3 film versus those in IGO.[18,22] This conclusion is further supported by XPS depth profile experiments carried out on In_2O_3/IGO bilayer films on Si/SiO_2 substrates. Composition changes for Ga, In, and Si clearly indicate vertical gradation going from the Ga-containing top layer to the bottom In_2O_3 film in contact with the SiO_2 interface (see the Supporting Information, Figure S3).

Additional evidence for a distinct IGO/In_2O_3 interface is evident in the cross-sectional TEM image of a bilayer TFT with a ~3 nm In_2O_3 layer and a ~10 nm IGO layer processed at 250 °C (Figure 3a inset). Clearly distinguishable from the IGO layer, the thinner In_2O_3 layer appears darker and is located close to the SiO_2 surface. These results suggest that significant diffusion of Ga atoms does not occur in the In_2O_3 layer under the exothermic combustion conditions. Interestingly, from the EF-NBD patterns of the In_2O_3/IGO bilayer shown in panels b and c in Figure 3, it can be seen that the former exhibits the characteristic diffraction pattern of a polycrystalline film (the detector resolution is 2 nm) whereas the upper IGO film

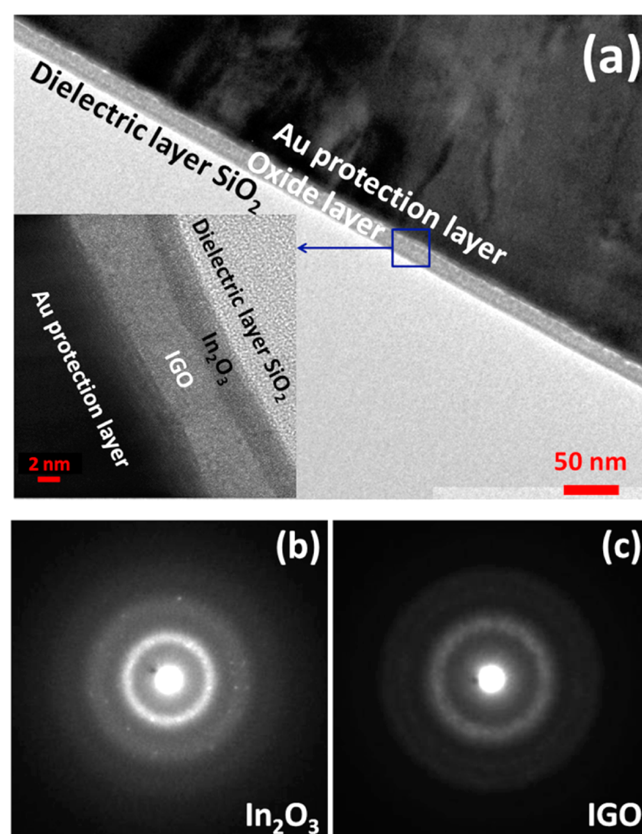


Figure 3. Microstructural characterization of bilayer TFTs. (a) High-resolution cross-sectional TEM image of In_2O_3 (3 nm)/IGO (10 nm) bilayer. (b, c) Diffraction patterns of In_2O_3 (3 nm) and IGO (10 nm) films. All films were annealed at 250 °C.

exhibits the typical "halo rings" of an amorphous material. Thus, all data confirm the bilayer nature of the channel region in these bMO FETs.

■ CONCLUSIONS

A fully solution-based, low-temperature-processed oxide bilayer TFT architecture has been realized via combustion chemistry, integrating high mobility ultrathin In_2O_3 as the lower channel layer and amorphous IGO as the upper layer in the channel. Such bilayer architectures address the low mobility of amorphous IGO TFTs fabricated at low temperature and the unsatisfactory high I_{off} and low I_{on}/I_{off} of single-layer In_2O_3 TFTs. The mobility and I_{on}/I_{off} ratio of our bilayer devices can reach ~2.56 $cm^2/(V\ s)$ and ~1 × 10^8, respectively, at a processing temperature of only 250 °C. The present strategy combining the advantages of ultrathin high mobility layer and an amorphous layer opens new opportunities for large-scale, high-performance, low-temperature solution-processable metal oxide TFTs.

■ ASSOCIATED CONTENT

Supporting Information

Associated content, including (a) AFM morphology, and (b) XPS spectra. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: t-marks@northwestern.edu (T.J.M.); a-facchetti@northwestern.edu (A.F.).

Notes

The authors declare no competing financial interest.

X.Y. and H.L. are on leave from University of Electronic Science and Technology of China

■ ACKNOWLEDGMENTS

We thank ONR (MURI N00014-11-1-0690), the Northwestern University Materials Research Science and Engineering Center (NSF DMR-1121262), and Polyera Corp. for support of this research. Microscopy studies were performed in the NIFTI and KECK II facilities of NUANCE Center at Northwestern University. NUANCE is supported by NSF-NSEC, NSF-MRSEC, Keck Foundation, the State of Illinois, and Northwestern University. X.Y. thanks the graduate student exchange program supported by the University of Electronic Science and Technology of China.

■ REFERENCES

(1) *Transparent Electronics: From Synthesis to Applications*; Facchetti, A.; Marks, T. J., Eds.; Wiley: Chichester, U.K., 2010.

(2) Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. *Nature* **2004**, *432*, 488−492.

(3) Dasgupt, S.; Kruk, R.; Mechau, N.; Hahn, H. *Nano Lett.* **2011**, *5*, 9628−9638.

(4) Kim, Y.-H.; Heo, J.-S.; Kim, T.-H.; Park, S.; Yoon, M.-H.; Kim, J.; Oh, M. S.; Yi, G. R.; Noh, Y.-Y.; Park, S. K. *Nature* **2012**, *249*, 128−132.

(5) Nasr, B.; Wang, D.; Kruk, R.; Rösner, H.; Hahn, H.; Dasgupta, S. *Adv. Funct. Mater.* **2013**, *23*, 1750−1758.

(6) Wang, L.; Yoon, M.-H.; Lu, G.; Yang, Y.; Facchetti, A.; Marks, T. J. *Nature* **2006**, *5*, 893−900.

(7) Jeong, J. K.; Jeong, J. H.; Choi, J. H.; Im, J. S.; Kim, S. H.; Yang, H. W.; Kang, K. N.; Kim, K. S.; Ahn, T. K.; Chung, H.-J.; Chung, H. K. *Dig. Tech. Pap.—Soc. Inf. Disp. Int. Symp.* **2008**, *39*, 1−4.

(8) Kim, D.-H.; Lu, N.; Ma, R.; Kim, Y.-S.; Kim, R.-H.; Wang, S.; Wu, J.; Won, S. M.; Tao, H.; Islam, A.; Yu, K. J.; Kim, T.-i.; Chowdhury, R.; Ying, M.; Xu, L.; Li, M.; Chung, H.-J.; Keum, H.; McCormick, M.; Liu, P.; Zhang, Y.-W.; Omenetto, F. G.; Huang, Y.; Coleman, T.; Rogers, J. A. *Science* **2011**, *333*, 838−843.

(9) Sun, J.; Zhang, B.; Katz, H. E. *Adv. Funct. Mater.* **2011**, *21*, 29−45.

(10) Zan, H.-W.; Yeh, C.-C.; Meng, H.-F.; Tsai, C.-C.; Chen, L.-H. *Adv. Mater.* **2012**, *24*, 3509−3514.

(11) Liu, J.; D. Buchholz, B.; Chang, R. P. H.; Facchetti, A.; Marks, T. J. *Adv. Mater.* **2010**, *22*, 2333−2337.

(12) Wang, L.; Yoon, M.-H.; Facchetti, A.; Marks, T. J. *Adv. Mater.* **2007**, *19*, 3252−3256.

(13) Bashir, A.; Wobkenberg, P. H.; Smith, J.; Ball, J. M.; Adamopoulos, G.; Bradley, D. D. C.; Anthopoulos, T. D. *Adv. Mater.* **2009**, *21*, 2226−2231.

(14) Faber, H.; Burkhardt, M.; Jedaa, A.; Kalblein, D.; Klauk, H.; Halik, M. *Adv. Mater.* **2009**, *21*, 3099−3104.

(15) Ha, Y.-G.; Emery, J. D.; Bedzyk, M. J.; Usta, H.; Facchetti, A.; Marks, T. J. *J. Am. Chem. Soc.* **2011**, *133*, 10239−10250.

(16) Lee, C.-G.; Dodabalapur, A. *Appl. Phys. Lett.* **2010**, *96*, 243501.

(17) Chiang, H. Q.; Wager, J. F.; Hoffman, R. L.; Jeong, J.; Keszler, D. A. *Appl. Phys. Lett.* **2005**, *86*, 013503.

(18) Pal, B. N.; Dhar, B. M.; See, K. C.; Katz, H. E. *Nat. Mater.* **2009**, *8*, 898−903.

(19) Presleya, R. E.; Honga, D.; Chianga, H. Q.; Hunga, C. M.; Hoffmanb, R. L.; Wagera, J. F. *Solid-State Electron.* **2006**, *50*, 500−503.

(20) Kim, J. B.; Fuentes-Hernandez, C.; Kim, S. J.; Choi, S.; Kippelen, B. *Organ. Electron.* **2010**, *11*, 1074−1078.

(21) Bae, C.; Kim, D.; Moon, S.; Choi, T.; Kim, Y.; Kim, B. S.; Lee, J.-S.; Shin, H.; Moon, J. *ACS Appl. Mater. Interfaces* **2010**, *2*, 626−632.

(22) Papadopoulos, T.; Cheun, H.; Kim, J.; Fenoll, M.; Dindar, A.; Haske, W.; Najafabadi, E.; Khan, T. M.; Sojoudi, H.; Barlow, S.; Graham, S.; Bredas, J. L.; Marder, S. R.; Kahn, A.; Kippelen, B. *Science* **2012**, *336*, 327−332.

(23) Kim, H.-S.; Park, J. S.; Jeong, H. K.; Son, K. S.; Kim, T. S.; Seon, J.-B.; Lee, E.; Chung, J. G.; Kim, D. H.; Ryu, M.; Lee, S. Y. *ACS Appl. Mater. Interfaces* **2012**, *4*, 5416−5421.

(24) Jeon, S.; Kim, S.; Park, S.; Song, I.; Park, J.; Kim, S.; Kim, C. *IEEE Electron Device Lett.* **2010**, *31*, 1128−1130.

(25) *Solution Processing of Inorganic Materials*; Mitzi, D. B., Ed.; John Wiley & Sons: Hoboken, NJ, 2008.

(26) Kim, M.-G; Kanatzidis, M. G.; Facchetti, A.; Marks, T. J. *Nat. Mater.* **2011**, *10*, 382.

(27) Hennek, J. W.; Kim, M.-G; Kanatzidis, M. G.; Facchetti, A.; Marks, T. J. *J. Am. Chem. Soc.* **2012**, *134*, 9593−9596.

(28) Fortunato, E.; Barquinha, P.; Martins, R. *Adv. Mater.* **2012**, *24*, 2945−2986.

(29) Matsuzaki, K.; Yanagi, H.; Kamiya, T.; Hiramatsu, H.; Nomura, K.; Hirano, M.; Hosono, H. *Appl. Phys. Lett.* **2006**, *88*, 092106.

(30) Jeong, S.; Ha, Y.-G.; Moon, H.; Facchetti, A.; Marks, T. J. *Adv. Mater.* **2010**, *22*, 1346−1350.

(31) Adamopoulos, G.; Bashir, A.; Thomas, S.; Gillin, W. P.; Georgakopoulos, S.; Shkunov, M.; Baklar, M. A.; Stingelin, N.; Maher, R. C.; Cohen, L. F.; Bradley, D. D. C.; Anthopoulos, T. D. *Adv. Mater.* **2010**, *22*, 4764−4769.

(32) Zhang, F. J.; Di, C. A.; Berdunov, N.; Hu, Y. Y.; Hu, Y. B.; Gao, X. K.; Meng, Q.; Sirringhaus, H.; Zhu, D. B. *Adv. Mater.* **2013**, *25*, 1401−1407.

(33) Yu, X. G.; Yu, J. S.; Zhou, J. L.; Wang, H.; Cheng, L. H.; Jiang, Y. D. *Jpn. J. Appl. Phys.* **2011**, *50*, 104101.

(34) Yu, X. G.; Yu, J. S.; Zhou, J. L.; Jiang, Y. D. *Appl. Phys. Lett.* **2011**, *99*, 063306.

(35) Ireland, R. M.; Dawidczyk, T. J.; Cottingham, P.; McQueen, T.; Johns, G.; Markovic, N.; Zhang, L. S.; Gopalan, P.; Katz, H. E. *ACS Appl. Mater. Interfaces* **2013**, *5*, 1604−1611.

(36) Fan, J. C. C.; Goodenough, J. B. *J. Appl. Phys.* **1997**, *48*, 3524.

(37) Moriga, T.; Kammler, D. R.; Mason, T. O. *J. Am. Ceram. Soc.* **1999**, *82*, 2705.
(38) Donley, C.; Dunphy, D.; Paine, D.; Carter, C.; Nebesny, K.; Lee, P.; Alloway, D.; Armstrong, N. R. *Langmuir* **2002**, *18*, 450.
(39) Banger, K. K.; Yamashita, Y.; Mori, K.; Peterson, R. L.; Leedham, T.; Rickard, J.; Sirringhaus, H. *Nat. Mater.* **2011**, *10*, 45−50.